1329582

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(19)

(54) SIGNAL TRANSLATING APPARATUS

(71) We, COMPAGNIE DES COMPTEURS, a French body corporation, of 42, rue Saint-Dominique, Paris (7 eme) France, and formerly of 3 rue Dosne, 75-Paris (16e), France, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to signal translating apparatus. The invention is particularly, but not exclusively, applicable to producing an output pulse train, the number of pulses in which is equal to the difference between the numbers of pulses in two input pulse trains. Such apparatus is particularly useful for producing an output signal whose mean recurrence frequency is equal to the difference between the recurrence frequencies of the input pulse trains, the input pulse signals representing for example physical quantities such as flow rates or angular velocities.

The invention provides frequency comparator apparatus for responding to the relative repetition rates of first and second signals in respective pulse trains and comprising separating means for separating in time said first and second signals, selective means having a first operational state in which it produces output pulse signals in response to said first signals and a second operational state in which it is inhibited from producing said output signals, and control means controlled by the separated signals and responsive to one of said second signals for setting said selective means to said second state and responsive to a subsequent one of said first signals for resetting said selective means to said first state.

Other features and advantages of the invention will be better understood from the following description of embodiments thereof, given by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a block diagram of frequency comparison apparatus in accordance with the invention; and

Figure 2 is a diagram showing various signals appearing in operation of the apparatus.

The frequency comparison apparatus shown in Figure 1 comprises a selective circuit comprising gate means 15 and 16 and a bistable trigger 12, and a control circuit comprising a bistable trigger 11 and an enabling circuit including a gate 13 and a differentiating circuit 14.

Two input pulse trains of frequencies f_1 and f_2 are received at the reference inputs E_1 and E_2 respectively of a circuit 10 enabling time separation of the pulses to be effected, preferably being a circuit of the type described in our French Patent 2064528, entitled "A circuit for separating and synchronising pulses". This circuit prevents the simultaneous application of pulses to the two inputs of the frequency comparator circuit proper and produces at terminals S_1 and S_2 signals whose number corresponds to that of the input signals but which are out of phase and synchronised respectively with a locally generated clock signal.

S_1 and S_2 are connected to the inputs of the first bistable trigger stage 11 which comprises two NAND-gates or invertor AND-gates, 11A, 11B, with two crossed inputs. The outputs of this trigger stage 11 are respectively connected to the inputs J and K of the second bistable trigger stage 12 which only actually changes state with the appearance of an enabling signal at an input D. This input D is connected to the terminals S_1 and S_2 through the medium of the NAND-gate 13 followed by the differentiating circuit 14, which serve as a delay circuit.

The second NAND-gate 15 with two inputs has its first input connected with the terminal S_1 through the inverter circuit 16 and its second input connected to the output Q of the trigger stage 12.

We shall now explain the operation of this comparator circuit on the basis of the assumption that the frequencies f_1 and f_2 are constant and such that $f_1 \geqslant f_2$. It will also be assumed that initially the trigger stage 11 is in the condition in which J=1, K=0 and

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the trigger stage 12 in the condition in which Q=1. Figure 2 plots the shape of the signals at various points in the circuit, as a function of time.

A negative pulse arriving at the input E_1 and reappearing at S_1, has no effect upon the trigger stage 11, which remains in the condition in which J=1. The trigger stage 12 therefore also remains biased into condition in which Q=1. The circuit 15 receiving the signal $\overline{S_1}(S_1=0, \overline{S_1}=1)$ and Q=1, at its inputs, produces at its output F the signal $\overline{\overline{S_1} \cdot Q}(\overline{S_1} \cdot Q=0)$ which is a negative pulse. In its turn, the circuit 13 produces the signal $\overline{S_1 \cdot S_2}$ which is a positive pulse; its trailing edge, differentiated by the circuit 14, appears at the output D in the form of a narrow delayed pulse, which, when applied to the trigger stage 12, leaves the latter in the condition in which Q=1, without making it charge state.

The input pulse at E_1 has thus been transmitted. If other pulses continue to be applied at E_1, a process identical to that described is repeated so that at the output F the same number of pulses appears at the input E_1, that is to say at the frequency f_1.

If, now, a pulse arrives at E_2, the reapperance of this pulse at S_2 produces a change in state of the trigger stage 11, into the condition in which J=0, K=1, thus biasing the inputs to the trigger stage 12 so that the subsequent arrival of the enabling pulse at its input D, will cause the stage 12 to change into a stage in which Q=0.

Until the arrival of the enabling pulse at the input D, the circuit 15 still receives the signal Q=1, but since $\overline{S_1}$ now has the complementary value $(\overline{S_1}=0)$, no pulse appears at the output F so that the input pulse at E_2 is not transmitted.

The circuits 13 and 14 produce the enabling pulse at D at the termination of the pulse from S_2, which enables the trigger stage 12 to be set to the condition in which Q=0, where it acts to block the circuit 15 vis-a-vis the next pulse to arrive at E_1.

The next pulse to arrive at E_1 will change the state in the trigger stage 11 back to the condition in which J=1, biasing the trigger stage 12 so that the subsequent arrival of the enabling pulse at its input D will cause it to be reset to the condition in which Q=1, but will not cause it to change state again. Thus, since the circuit 15 receives the signal $\overline{S_1}$ with the initial value $\overline{S_1}=1$ but with Q=0, it does not transmit this input pulse so that the latter is consequently subtracted from the chain f_1.

When the delayed differentiation pulse obtained at D enables the trigger stage 12 to be reset to condition in which Q=1, the system is restored to the initial condition.

Since we have assumed that $f_1 \gg f_2$ applies, no more than one pulse can appear at E_2 between two pulses at E_1. It will be seen, therefore, that each pulse at E_2, not itself transmitted, has the effect of inhibiting the transmission of the next pulse at E_1. The signal picked up at the output F is thus truly representative of the frequency difference $f_1 - f_2$, whatever the ratio $f_1/f_2 \gg 1$.

This comparator circuit can be supplemented as shown in broken lines in order to make it symmetrical, by the addition of a NAND-gate 15' with two inputs, one connected to the output $\overline{Q}$ of the trigger stage 12 and the other to the output S_2 through the medium of an invertor circuit 16'. If the condition $F_2 > f_1$ applies, we then obtain at the output F' a signal representing the frequency difference $f_2 - f_1$, whatever the ratio

$$\frac{f_2}{f_1} \gg 1.$$

A supplementary arrangement provides for the connection of the two outputs F and F' to the inputs of a NAND-gate 17. This makes it possible to detect parasitic pulses present in the two channels, in respect of pulses which are of the same frequency but are out of phase in the channels E_1 and E_2, and in the absence of the circuit 10, since as a rule $f_1 - f_2 = 0$.

Since the circuit simply contains logic elements, it can be manufactured equally well using electronic, fluidic or other components.

The invention is applicable to the comparison of the recurrence frequencies of two periodic signals which can represent physical quantities converted into proportional frequencies.

WHAT WE CLAIM IS:—

1. Frequency comparator apparatus for responding to the relative repetition rates of first and second signals in respective pulse trains and comprising separating means for separating in time said first and second signals, selective means having a first operational state in which it produces output pulse signals in response to said first signals and a second operational state in which it is inhibited from producing said output signals, and control means controlled by the separated signals and responsive to one of said second signals for setting said selective means to said second state and responsive to a subsequent one of said first signals for resetting said selective means to said first state.

2. Apparatus in accordance with claim 1

wherein said selective means comprises gate means for passing said first signals selectively in response to a gate signal and bistable means for selectively producing said gate signals in said first state of said selective means.

3. Apparatus in accordance with claim 2 wherein said bistable means has first and second inputs and an enabling input and is enabled to change state in response to a change in first and second control signals on said first and second inputs by an enabling signal on said enabling input, said control means being arranged to provide said first and second control signals and said enabling signal.

4. Apparatus in accordance with any preceding claim wherein said selective means is arranged to produce further output pulse signals in response to said second signals when in said second state and to be inhibited from producing said further output signals when in said first state.

5. Apparatus in accordance with claim 4 as appendant to claim 2 wherein said selective means includes further gate means for passing said second signals selectively in response to a further gate signal, and said bistable means is arranged to produce said further gate signal selectively in said second state of said selective means.

6. Apparatus in accordance with claim 4 or 5 and including NAND gate means responsive to the first said output signals and said further output signals.

7. Apparatus in accordance with any preceding claim wherein said control means includes control bistable means having first and second operational states which it assumes in response to said first signals and said second signals respectively, and enabling means responsive to terminations of said first and second signals for enabling said selective means to respond to a change of state of said control bistable means.

8. Apparatus in accordance with claim 7 as appendant to claim 3 wherein said control bistable means is arranged to provide said first and second control signals in its first and second states respectively and said enabling means is arranged to provide said enabling signals.

9. Apparatus in accordance with claim 7 or 8 wherein said enabling means includes means for producing third signals in response to each of said first and second signals, and means responsive to the termination of each of said third signals.

10. Apparatus in accordance with claim 9 wherein said means for producing third signals includes a NAND gate, and said means responsive to the termination includes a differentiating circuit.

11. Frequency comparison apparatus substantially as herein described with reference to the accompanying drawings.

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Sheet 1

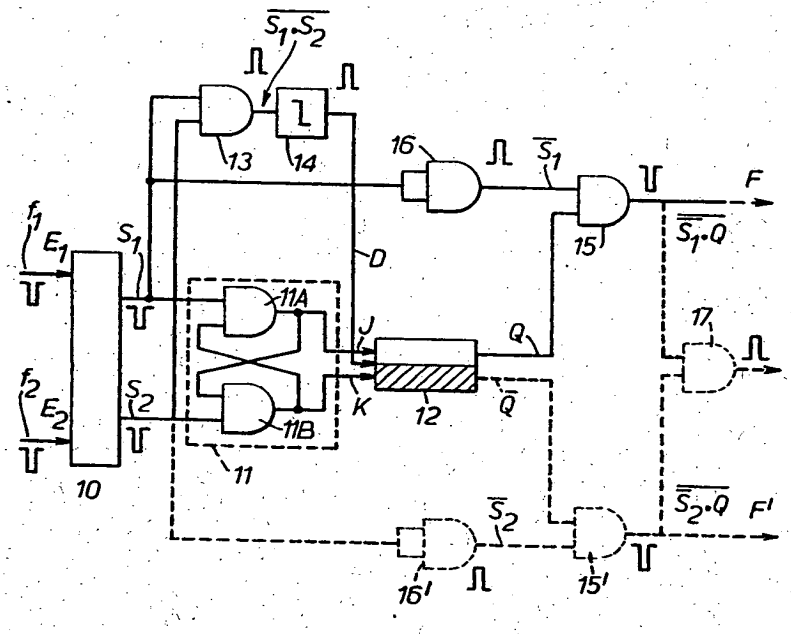

FIG. 1.

1329582 COMPLETE SPECIFICATION
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Sheet 2

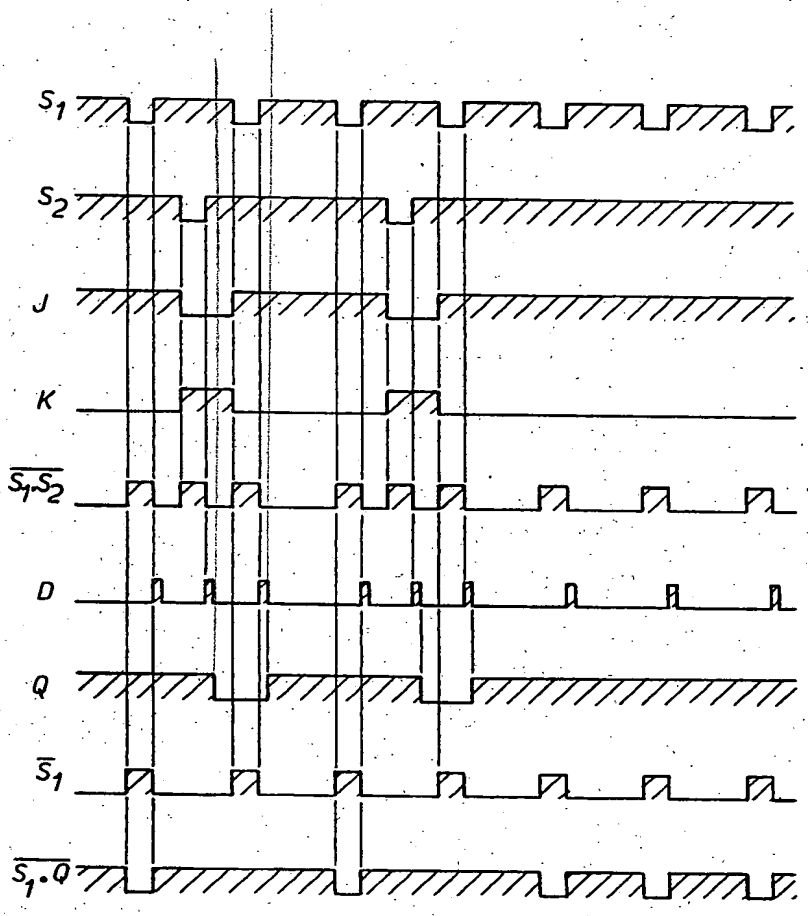

FIG. 2.